IN THE SPECIFICATION:

Please amend the following paragraphs as indicated:

[0038] The bus control logic 400 generally controls the manner in which the packets are read from the input and insert packet buffers 104, 112. The reading process is generally conducted in three ~~phase~~ phases. The host processor's ISR signal is divided into 94 read slots, and each read slot is divided into three time domain multiplexed phases. Each phase contains one read cycle form the packet buffer 104. The first phase includes the reading of data other than the packet data itself (e.g., timestamps, PID value, page number, PCR flag, CMP packet data). The second and third phases are used to read data stored in the packet buffers. These phases will be described in greater detail below.

[0051] Software in the host processor 114 checks the fullness of the input packet buffers for any violations of re-multiplexer packet jitter specifications. If the input packet buffer 104 is filled to a predetermined level, the packets stored in the input buffers 104 are assumed to be corrupted. The re-multiplexing software may also check for other error conditions and can instruct the output processor to set the transport error indicator bit in the MPEG header in all packets associated with any one of the outputs ~~[why?]~~. Once the error condition has been resolved, the software will instruct the output processor 124 to resume normal packet processing once the error condition has been resolved.

[0056] As mentioned above, the output processor 414 includes a time reference generator 424. The output processor's time reference generator 420 is the same as the time generator in the input processor except that the output processor time reference generator acts

as the master counter that controls synchronization between the output processor 414 and the input processor. In one example, when the output processor's time reference generator 424 reaches a terminal count, it sends a synchronization load pulse to slave counters in the input processor 120 to reload all of the counters with 0's. The output timestamp is sampled when the first word is read from the FIFO.